AMENDMENT TO THE SPECIFICATION

Please amend the paragraph beginning on page 9, line 2 as set forth below:

It is noted that system 10 (and more particularly processors 12A-12B, L2 cache 14, memory controller 16, I/O interfaces 22A-22D, I/O bridges 20A-20B and bus 24) may be integrated onto a single integrated circuit as a system on a chip configuration. In another configuration, memory 26 may be integrated as well. Alternatively, one or more of the components may be implemented as separate integrated circuits, or all components may be separate integrated circuits, as desired. Any level of integration may be used.

Please amend the paragraph beginning on page 9, line 20 as set forth below:

Turning next to Fig. 2, a timing diagram is shown illustrating transmission and sampling of signals according to one embodiment of system 10 and bus 24. Other embodiments are possible and contemplated. The clock signal on clock line(s) ~~26~~ 36 is illustrated (CLK) in Fig. 2. The high and low portions of the clock signal CLK are delimited with vertical dashed lines.

Please amend the paragraph beginning on page 17, line 8 as set forth below:

Turning next to Fig. 5, a block diagram illustrating exemplary signals which may be included on address bus 30 is shown. Other embodiments are possible and contemplated. In the illustrated embodiment, address bus 30 includes address lines used to provide the address of the transaction (Addr[39:5]) and a set of byte enables (A_BYEN[31:0]) indicating which bytes on the data bus 34 are being read or written during the transaction, a command (A_CMD[2:0]) used to indicate the transaction to be performed (read, write, etc.), a transaction ID (A_ID[9:0]) used to identify the transaction, and a set of attributes (A_ATTR[n:0]).

Please amend the paragraph beginning on page 18, line 3 as set forth below:

Turning next to Fig. 6, a block diagram illustrating exemplary signals which may be employed on one embodiment of response lines 32 is shown. Other embodiments are possible and contemplated. In the embodiment of Fig. 6, response lines 32 include a set of shared signals (R_SHD[5:0]) and a set of exclusive signals (R_EXC[5:0]). Each agent which participates in coherency may be assigned a corresponding one of the set of shared signals and a corresponding one of the set of exclusive signals. The agent may report shared ownership of the data affected by a transaction by asserting its shared signal. The agent may report exclusive ownership of the data affected by a transaction by asserting its exclusive signal. The agent may report no ownership of the data by not asserting other signal. In the illustrated embodiment, modified ownership is treated as exclusive. Other embodiments may employ a modified signal (or an encoding of signals) to indicate modified.

Please amend the paragraph beginning on page 20, line 13 as set forth below:

Generally, the database of system 10 carried on carrier medium ~~120~~ 300 may be a database which can be read by a program and used, directly or indirectly, to fabricate the hardware comprising system 10. For example, the database may be a behavioral-level description or register-transfer level (RTL) description of the hardware functionality in a high level design language (HDL) such as Verilog or VHDL. The description may be read by a synthesis tool which may synthesize the description to produce a netlist comprising a list of gates from a synthesis library. The netlist comprises a set of gates which also represent the functionality of the hardware comprising system 10. The netlist may then be placed and routed to produce a data set describing geometric shapes to be applied to masks. The masks may then be used in various semiconductor fabrication steps to produce a semiconductor circuit or circuits corresponding to system 10. Alternatively, the database on carrier medium 300 may be the netlist (with or without the synthesis library) or the data set, as desired.